MCS6530-004 (TIM)

SOFTWARE DEVELOPMENT AID

TIM is the Terminal Interface Monitor program for MOS TECHNOLOGY, INC.'s MCS650X microprocessors. It is supplied in read-only memory (ROM) as part of the MCS6530 multi-function chip. Because the TIM code is non volatile, it is available at system power-on and cannot be destroyed inadvertently by user programs. Furthermore, the user is free to selectively use only those TIM capabilities which he needs for a particular program. Both interrupt types, interrupt request (IRQ) and non-maskable interrupt (NMI) may be set to transfer control to TIM or directly to the user's program.

TIM communicates with the user via a serial full-duplex port (using ASCII codes) and automatically adjusts to the speed of the user's terminal. Any speed... even non-standard ones...can be accommodated. If the user's terminal has a long carriage return time, TIM can be set to perform the proper delay. Commands typed at the terminal can direct TIM to start a program, display or alter registers and memory locations, set breakpoints, and load or punch programs. If available in the system configuration, a high-speed paper tape reader may be used to load programs through a parallel port on the MCS6530 chip. Programs may be punched in either of two formats -- hexadecimal (assembler output) of BNPF (which is used for programming read-only memories). On loading or modifying memory, TIM performs automatic read-after-write verification to insure that addressed memory exists, is read-write type, and is responding correctly. Operator errors and certain hardware failures may thus be detected using TIM.

TIM also provides several subroutines which may be called by user programs. These include reading and writing characters on the terminal, typing a byte in hexadecimal, reading from high-speed paper tape, and typing a carriage-return, line-feed sequence with proper delay for the carriage of the terminal being used. Program tapes loaded by TIM may also specify a start address so that programs may be started with a minimum of operator action.

TIM is normally entered when a 'BRK' instruction is encountered during program execution. At that time CPU registers are output: * PC F A X Y S and control is given to the terminal.

Note: PC = Program Counter
F = Processor Status Register
A = Accumulator
X = Index Register, X
Y = Index Register, Y
S = Stack Pointer

In summary, TIM's features include the following capabilities:

- Self adapting to any terminal speed for 10-30 cps
- Display and Alter CPU registers
- Display and Alter Memory locations
- Read and Write/Punch hex formatted data

- Write/Punch BNPF format data for PROM programmers
- Unlimited breakpoint capability
- Separate non-maskable interrupt entry and identification
- External device interrupts directable to any user location or defaulted to TIM recognition
- Capability to begin or resume execution at any location in memory
- Completely protected, resident in Read-Only Memory
- Capability to bypass TIM entirely to permit full user program control over system
- High speed 8-bit parallel input option
- User callable I/O subroutines

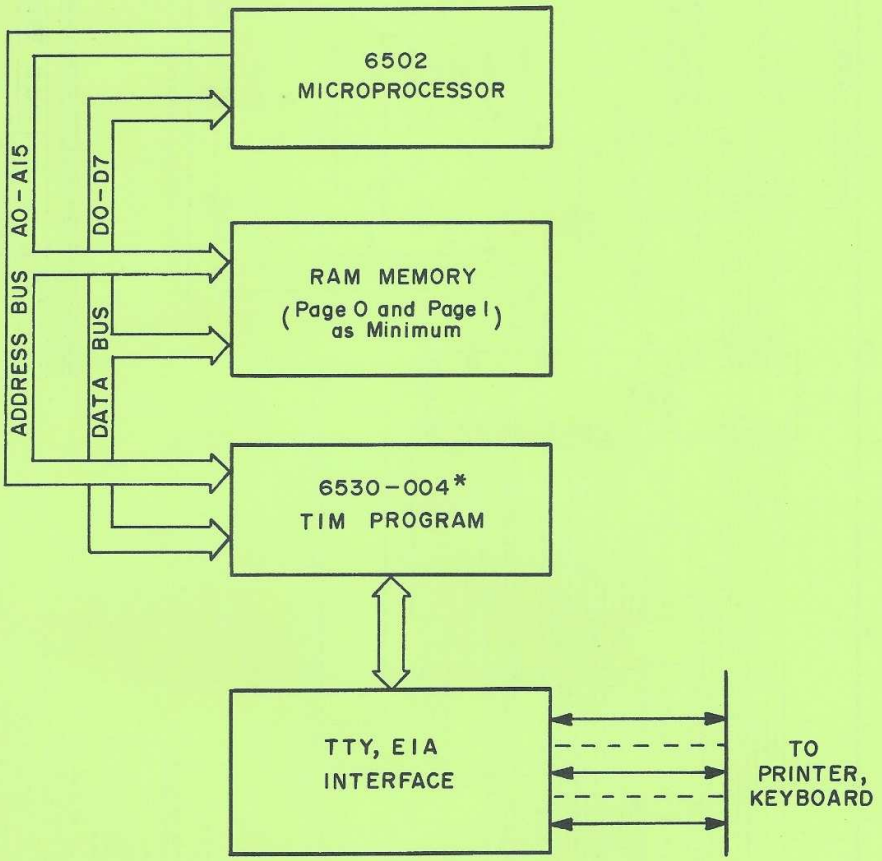
The commands used for directing TIM to perform these functions have been held to a minimum. This means that TIM is easily learned and readily remembered. TIM's Command Set consists of:

.R	Display registers (PC, F, A, X, Y, S)
.M ADDR	Display memory (8 bytes beginning at ADDR)
.: DATA	Alters perviously displayed item
.LH	Load Hexadecimal tape
.WB ADDR1, ADDR2	Write BNPF tape (from ADDR1 to ADDR2)
.WH ADDR1, ADDR2	Write hex tape (from ADDR1 to ADDR2)
.G	Go, continue execution from current PC address
.H	Toggles high-speed-reader option (if its on, turns it off; if off, turns on)

TIM is offered in the form of a 1K x 8 program resident in the MCS6530-004 at a 1 to 99 price of $30.00

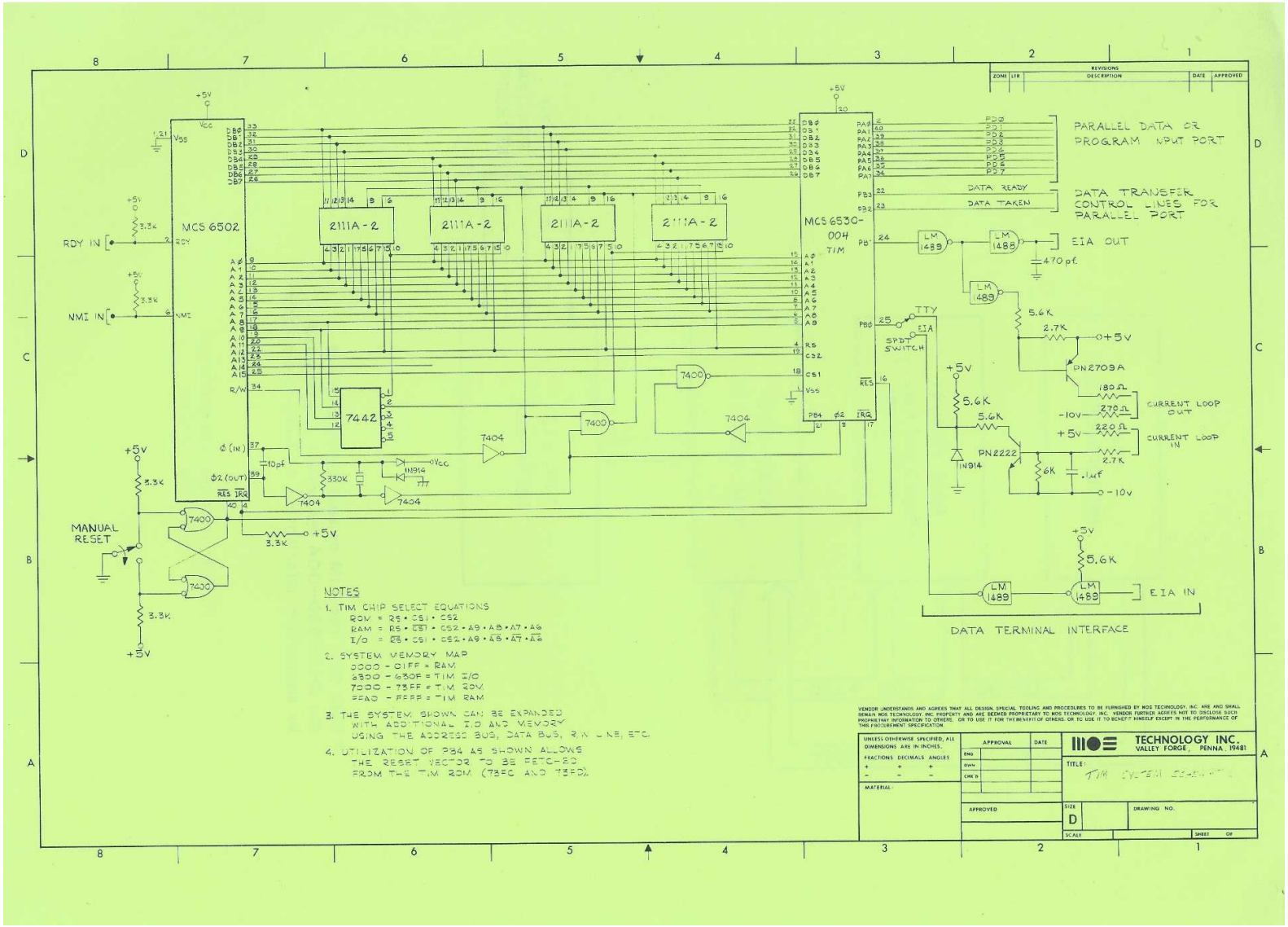
The TIM unit comes with:

1 - MCS6530-004 Multi-function Chip
1 - TIM Users Manual
1 - TIM System Schematic



* Note that the TIM as sold consists only of the MCS6530-004 component accompanied by supporting information to build this system

TYPICAL MINIMUM CONFIGURATION
FOR "TIM" SYSTEM


MCS 6502
2111A-2
2111A-2
2111A-2
2111A-2
MCS 6530-004 TIM
7442
7400
7404
RDY IN
NMI IN
MANUAL RESET
3.3K
10pf
330K
IN914
Φ (IN)
Φ2 (OUT)
R/W
RES
IRQ
PARALLEL DATA OR PROGRAM INPUT PORT
DATA READY
DATA TAKEN
DATA TRANSFER CONTROL LINES FOR PARALLEL PORT
EIA OUT
470 pf.
LM 1489
LM 1488
TTY
EIA
SPDT SWITCH
5.6K
2.7K
PN2709A
180Ω
270Ω
330Ω
CURRENT LOOP OUT
CURRENT LOOP IN
PN2222
6K
.1mf
-10v
+5v
EIA IN
DATA TERMINAL INTERFACE
NOTES
1. TIM CHIP SELECT EQUATIONS
ROM = RS • CS1 • CS2
RAM = RS • CS1 • CS2 • A9 • A8 • A7 • A6
I/O = RS • CS1 • CS2 • A9 • A8 • A7 • A6
2. SYSTEM MEMORY MAP
0000 - 01FF = RAM
6300 - 630F = TIM I/O
7000 - 73FF = T.M. ROM
FFA0 - FFFF = TIM RAM
3. THE SYSTEM SHOWN CAN BE EXPANDED WITH ADDITIONAL I/O AND MEMORY USING THE ADDRESS BUS, DATA BUS, R/W LINE, ETC.
4. UTILIZATION OF PB4 AS SHOWN ALLOWS THE RESET VECTOR TO BE FETCHED FROM THE TIM ROM (73FC AND 73FD).
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
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UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES.
FRACTIONS DECIMALS ANGLES
MATERIAL
APPROVAL DATE
ENG
DWN
CHK'D
APPROVED
MOS TECHNOLOGY INC.
VALLEY FORGE, PENNA. 19481
TITLE: TIM SYSTEM SCHEMATIC
SIZE D
DRAWING NO.
SCALE
SHEET OF